Comparison between Symmetrical and Asymmetrical Single Phase Seven Level Cascade H-Bridge Multilevel Inverter with PWM Topology

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***Abstract*---In this paper, a different configuration based on different DC bus voltage for a cascade H-Bridge multilevel inverter has been presented. Two different symmetrical and asymmetrical arrangements of a seven-level cascade H-Bridge inverters have been compared, in order to find an optimum arrangement with lower switching losses and optimized output voltage quality. The optimized asymmetrical arrangement has been compared with a conventional seven-level inverter. The comparison results show that an asymmetrical configuration can obtain more voltage levels in output voltage with same number of component compared with the conventional seven-level inverter and this will lead to the reduction of harmonic content of output voltage. A predictive current control technique has been carried out to verify the viability of new configuration. The advantages of this control method are simplicity and applicability for n-level multilevel inverters, without a significant change in the control circuit.**

***Keywords*---** Asymmetric Multilevel Inverter, Unipolar ISPWM, THD and Switching Loss

I. INTRODUCTION

The switching frequency is restricted by switching losses in high power and high voltage applications, multilevel inverters have found wide acceptance as they can achieve a low harmonic component with low switching frequency. Furthermore, low blocking voltage by switching devices is the other advantage of this type of converters as well as minimum harmonic distortion and switching losses. Multilevel inverters are mainly utilized to synthesize a desired voltage wave shape from several levels of dc voltages. Their main advantaged are low harmonic distortion of the generated output voltage, low electromagnetic emissions, high efficiency capability to operate at high voltages and modularity. Three topologies have been reported for multilevel inverters: Diode- clamped, flying capacitor and cascaded H-bridge [4].The topology considered for this work is the cascaded H-bridge inverter which requires several independent dc sources. Normally, each phase of a cascaded multilevel inverter requires "n" dc sources for 2n+1 level. For many applications, multiple dc sources are required demanding long cables and this could lead to voltage unbalance among the dc sources. With an aim to reduce the number of dc sources required for the cascaded multilevel inverter for a motor drive, this paper focuses on comparison between symmetric and asymmetric cascade MLI that uses equal and unequal dc sources in each phase to generate a seven level equal step multilevel output [5]. This structure is favorable for high power applications since it provides higher voltage at higher modulation frequencies (where they are needed) with a low switching Implementation and Control of Variable Frequency ISPWM Technique for an Asymmetric Multilevel Inverter (carrier) frequency. It means low switching loss for the same total harmonic distortion (THD). It also improves the reliability by reducing the number of dc sources when comparing symmetrical H-Bridge MLI. For the cascaded multilevel inverter there are several well known sinusoidal pulse width modulation strategies [1].Compared to the conventional triangular carrier based PWM, the inverted rectified sine carrier PWM has a better spectral quality and a higher fundamental output voltage without any pulse dropping [2]. However, the fixed frequency carrier based PWM affects the switch utilization in multilevel inverters. In order to balance the switching duty among the various levels in inverters, a variable frequency carrier based PWM has been suggested [3]. The VAISPWM provides an enhanced fundamental voltage, lower total harmonic distortion (THD) and minimizes the switch utilization among the various levels in inverters. In this method the control signals have been generated by comparing sinusoidal reference signal with a high frequency inverted sine carrier. The carrier frequencies are so selected that the number of switching in each band are equal. The proposed modulation technique maximizes the output voltage and gives a low THD of 21.5%. A comparative evaluation between the VAISPWM and the conventional modulation is also presented in terms of output voltage quality, power circuitry complexity, and total harmonic distortion (THD), Both the MLI circuit topology and its new control scheme are described in detail and their performance is verified based on simulation and experimental results.

II. SYMMETRICAL AND ASYMMETRICAL SEVEN-LEVEL CASCADE H-BRIDGE INVERTER

A. Symmetrical DC Link Voltage Configuration

Structure of seven-level single-phase cascade H-Bridge inverter. In conventional structure DC link voltage is shared equally among the three DC voltage sources should be regulated to the equal value at V/3 if DC voltage across three voltage sources is boosted to V_{dc}. shows all possible switching states with relative output voltage levels in

conventional arrangement fig.1. As it is clear seven output voltage levels can be generated based on different switching states. Fig.1 depicted the adjacency of switching states regarding to switching states which shows all output voltage level of single-phase conventional topology. As it shown, adjacency is available between all switching states as it is possible to move from one level to other one with one switching change.

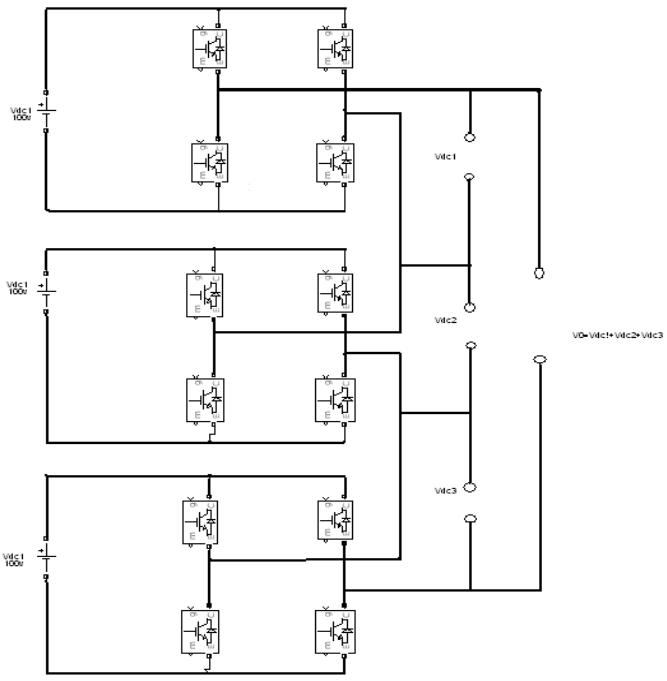

Fig.1: Symmetrical seven level configuration

B. Asymmetric Cascaded Multilevel Inverter

The seven - level cascaded multilevel inverter consists of two H-Bridges. The first H-Bridge H_1 consists of a separate DC source V_{dc}, whereas the second H-Bridge H_2 consists of a dc source $V_{dc}/2$ as shown in Fig.2. Let the output of H-Bridge-1 be denoted as $V_1(t)$ and the output of H-Bridge-2 be denoted as $V_2(t)$. Hence the total output voltage is given by $V(t)=V_1(t)+V_2(t)$. By alternately opening and closing the switches S_1,S_4 and S_2,S_3 of H-Bridge-1 appropriately, output of H1 $V_1(t)$ can be made equal to $+V_{dc}$, 0 or $-V_{dc}$. Similarly the output voltage of H-Bridge-2 $V_2(t)$ can be made equal to $-V_{dc}/2$, 0 or $+V_{dc}/2$ by opening and closing the switches of H_2 [6]. Hence V(t) takes values $-3/2V_{dc}$, $-V_{dc}$, $-1/2V_{dc}$, 0, $+1/2V_{dc}$, $+V_{dc}$, $+3/2V_{dc}$ as shown in the Fig.3.

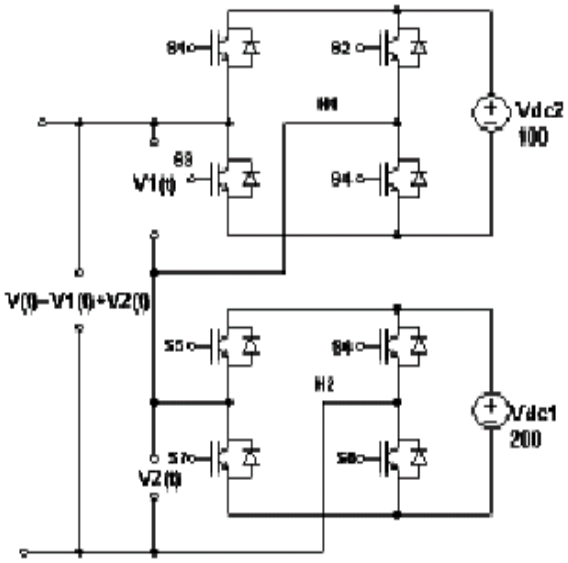

Fig 2: Asymmetric Cascaded Multilevel Inverter

The advantages of the topology are:

• Reduced number of dc sources.

• High speed capability

• Low switching loss

• High conversion efficiency.

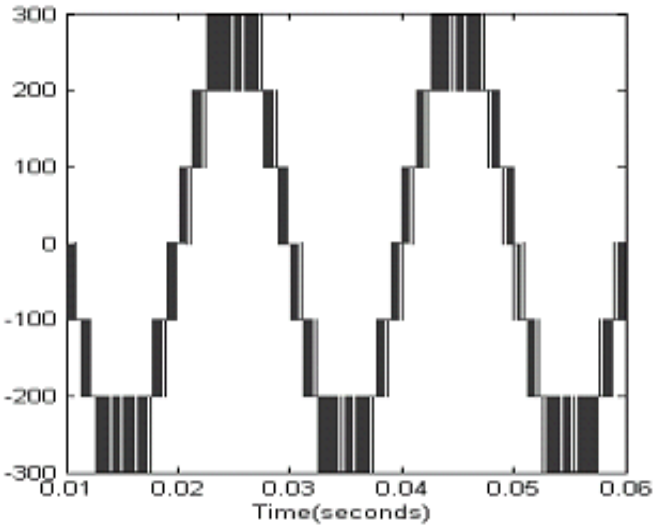

Fig 3: Output Voltage Waveform of Asymmetric Cascaded Seven Level Inverter.

III. PROPOSED VARIABLE AMPLITUDE INVERTED SINE PWM TECHNIQUE (VAISPWM)

The proposed control strategy replaces the conventional fixed Amplitude carrier waveform [7] by variable frequency inverted sine wave. The inverted sine PWM has a better

spectral quality and a higher fundamental voltage compared to the triangular based PWM. But the main drawback is the marginal boost in the magnitude of lower order harmonics and unbalanced switch utilization. This is overcome by employing variable Amplitude inverted sine carrier signals. In order to balance the number of active switching among the levels is to vary the carrier frequency based on the slope of the modulating wave in each band. The frequency ratio for each band should be set properly for balancing the switching action for all levels. The reference carrier frequency was chosen as 1050Hz as switching losses and THD both are low as shown in Fig.4.

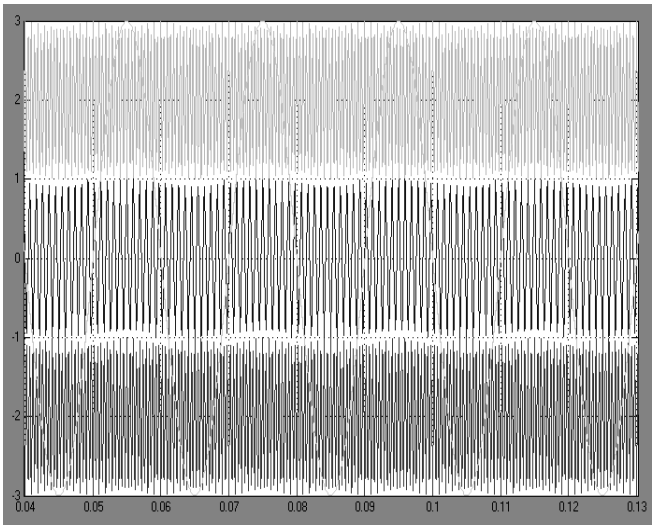

Fig.4: Generation Carrie Waves for proposed PWM VAISPWM

IV. PROPOSED UNIPOLAR INVERTED SINE PWM FOR HYBRID MULTILEVEL INVERTER

The proposed unipolar control strategy replaces the triangular based carrier waveform by inverted sine wave. The inverted sine PWM has a better spectral quality and a higher fundamental voltage compared to the triangular based PWM. The application of unipolar PWM to inverted sine carrier results in the reduction of carrier frequencies or its multiples and significant reduction in switching losses. So, the advantage of inverted sine and unipolar PWM are combined to improve the performance of the hybrid multilevel inverter. The inverted sine carrier PWM (ISCPWM) method uses the sine wave as reference signal while the carrier signal is an inverted (high frequency) sine carrier that helps to maximize the output voltage for a given modulation index. From the Fig.5. It is clear that the pulses are generated whenever the amplitude of the reference sine wave is greater than that of the inverted sine carrier wave.

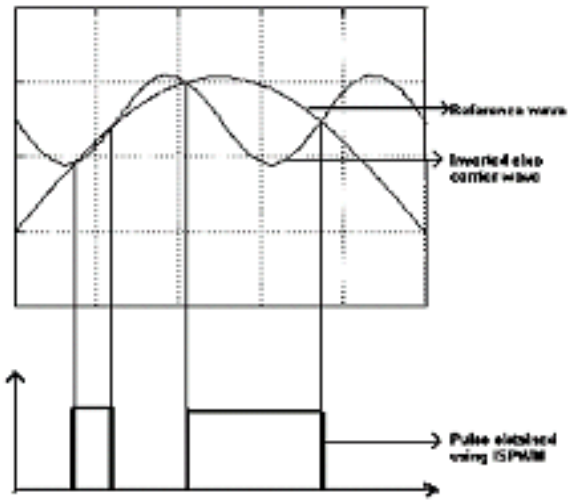

Fig .5. Generation of pulse using ISPWM

• It has a better spectral quality and a higher fundamental component compared to the conventional sinusoidal PWM (SPWM) without any pulse dropping.

• The ISCPWM strategy enhances the fundamental output voltage particularly at lower modulation index ranges.

• There is a reduction in the total harmonic distortion (THD) and switching losses.

• The appreciable improvement in the total harmonic distortion in the lower range of modulation index attracts drive applications where low speed operation is required.

• Harmonics of carrier frequencies or its multiples are not produced.

V. SWITCHING LOSS CALCULATION FOR THE MAIN SWITCH IGBT AND ANTI PARALLEL DIODE

The equations governing the calculation of switching loss for an IGBT and diode are given below and the switching energy is obtained from the area under the power curve [8, 9]. The equations governing the switching loss is given by

$$E_{on} = \int_0^{t_{on}} P(t) \cdot dt \qquad (1)$$

$$E_{off} = \int_0^{t_{off}} P(t) \cdot dt \qquad (2)$$

$$E_{SW} = E_{on} + E_{off} \qquad (3)$$

$$E_{on} = \frac{1}{2} V_{CE} \cdot I_C \cdot (t_{on} + t_{off}) \qquad (4)$$

The switching loss [13] of an IGBT is calculated from the equation

$$P_{SW} = f_{SW} \cdot E_{SW} \qquad (5)$$

The switching loss of the diode is calculated from the equation

$$P_{SW}D = \frac{1}{2}V_D \cdot I_D \cdot (t_{on} + t_{off}) \cdot f_{SW} \quad (6)$$

The voltage, current, power waveforms and the variation of switching loss with frequency is shown in the following figures.

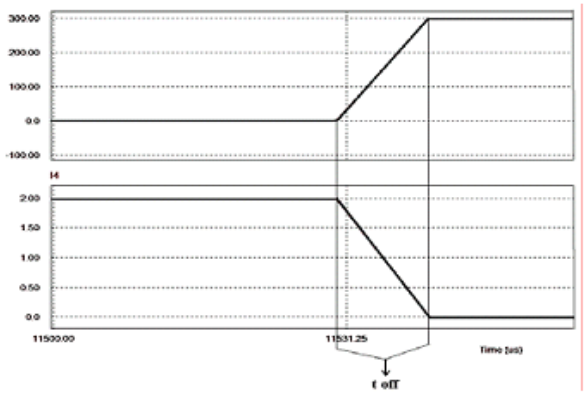

Fig.6. Determination of turn -off time

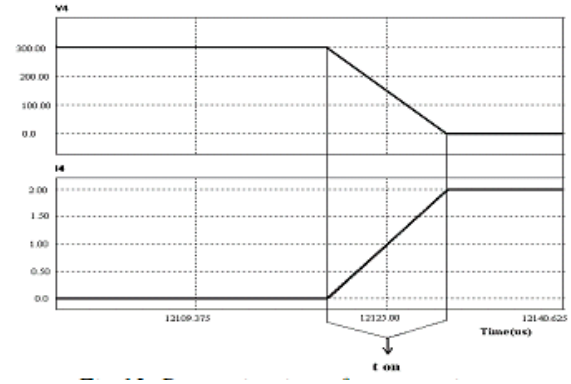

Fig.7. Determination of turn -on time

VI. SIMULATON RESULTS

The comparison of symmetrical and asymmetrical of an inverted sine pulse-width modulated for single-phase cascade multilevel inverter with symmetrical multilevel inverter output voltage as shown in fig .9. And the gating pulse is shown in fig.8. And also THD for symmetrical MLI as shown in fig.10. It is worth mentioning that the output of an all bridges will be equal. A SMLI captains three series-connected 100V. Simulations have been carried out in MATLAB-SIMULINK. But in comparing to the asymmetrical cascade H-bridge MLI will gives the same seven level output as shown in Fig. 12. When compared to symmetrical H-bridge MLI. The gating pulse of an asymmetrical multilevel inverter as shown in fig.11. And THD is as shown in fig.13. In the asymmetrical cascade multilevel inverter will gives the different voltages for each bridges, for the first bridge will gives the input of 100V and the another bridge will gives the 200V then output of total bridge will gives the 300V, when comparing to the symmetrical H-bridge the results of both output voltages and FFT analysis are verified by simulating the both the circuit using MATLAB

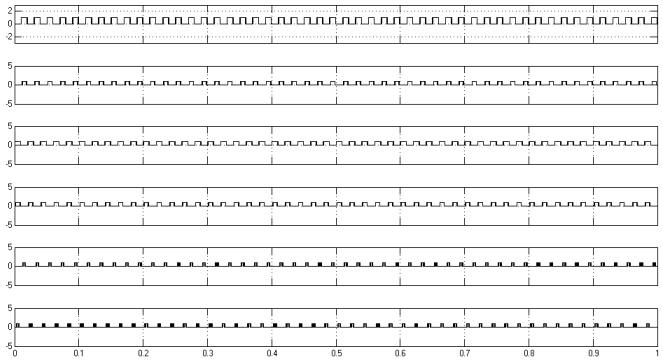

Fig 8. Generation of gating pulses for symmetrical H-Bridge inverter

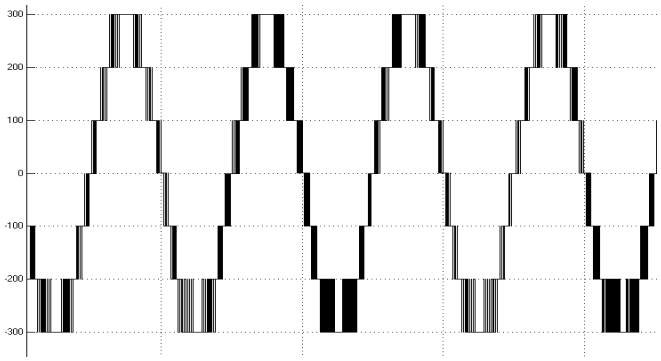

Fig.9. output voltage for Symmetrical H-bridge

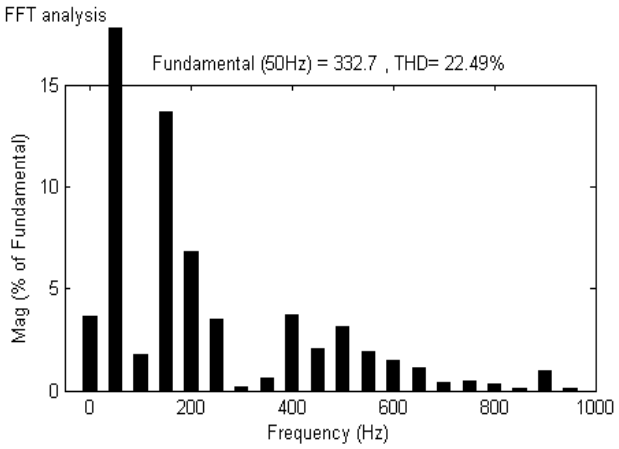

Fig.10. Total harmonic distortion for symmetrical cascade inverter

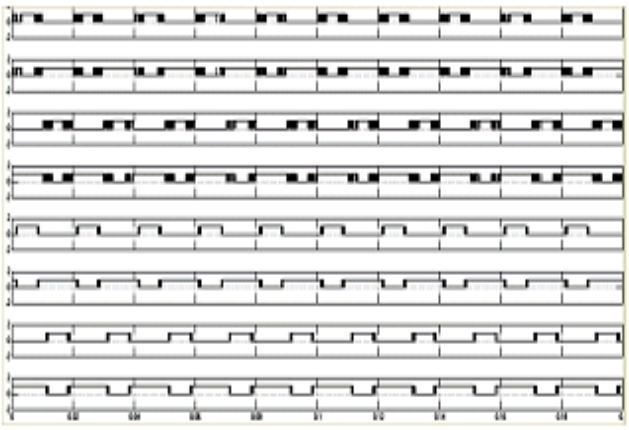

Fig 11. Generation of gating pulses for asymmetrical H-Bridge inverter

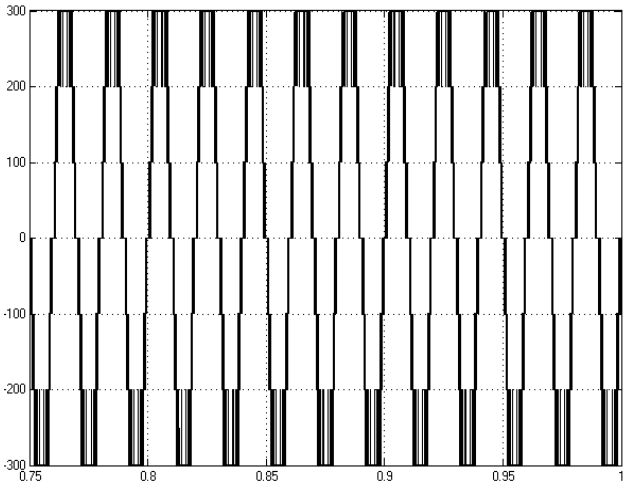

Fig.12. output voltage for Asymmetrical H-bridge

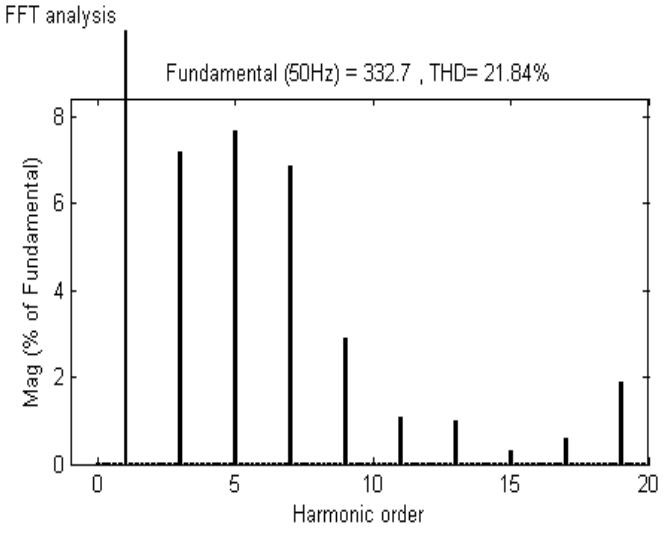

Fig.13. Total harmonic distortion for asymmetrical cascade inverter

VII. CONCLUSIONS

This paper presented a comparison between single phase seven levels H-bridge Inverter, which uses equal DC sources and symmetrical MLI and different DC sources an asymmetrical MLI, is used as load to observe the performance output voltages. The proposed ISPWM will give the FFT Analysis THD values 21.84 voltage of 332.7 V. So that the number of bridges and DC sources and also THD, switching losses are reduced. When compared to symmetrical MLI. Simulations have been carried out in MATLAB-SIMULINK to study the performance of the proposed prototype.

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