A 1.5v CMOS Fuzzifier

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***Abstract*— A versatile low-voltage CMOS Fuzzifier circuit with a trapezoidal transconductance characteristic and independently programmable slope, height and horizontal position is designed in 0.35µm standard CMOS technology. Simulation results using HSPICE and level 49 parameters (BSIM3v3) that verify the functionality of circuit with 1.5 V supply are presented.**

***Keywords*—** Fuzzifier, Transconductor, Low-voltage, Low-power and Fuzzy

I. INTRODUCTION

Zadeh proposed in 1965 a logic with fuzzy truth, connection and rules of inference, which was named Fuzzy logic. This approach has been successfully applied in many fields, like automatic process control and expert system and pattern recognition.

The fundamental operation in fuzzy logic is fuzzification which consists of the determination of the degree of association of a variable to a fuzzy set and is implemented by means of fuzzifier. This circuit provides a nonlinear relation that measures the compatibility of an object with the concept represented by a fuzzy set. Usually, fuzzifiers have a triangular or trapezoidal shape and, in order to guarantee general application, it needs to have programmable parameters (horizontal position, height, width and edge slope) (Fig. 1).

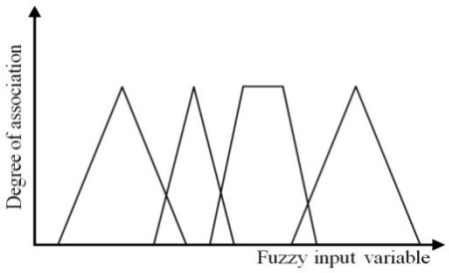

Fig. 1. Fuzzification of an input variable using membership function

For designing Fuzzifiers three generally methods exist; voltage-mode, current-mode and transconductance-mode circuits. Input and output signals are voltages in voltage-mode circuits and currents in current-mode circuits. Transconductance-mode circuits have a voltage input signal and a current output signal.

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Since fuzzifier is a first circuit in fuzzy controllers (Fig. 2), Transconductance mode is the best choice for designing a fuzzifier. This is due to the fact that output currents from transconductance mode MFGC are easily added, or processed using MAX, MIN and multiplier nonlinear operators in subsequent aggregation and defuzzification stages of fuzzy system. At the same time, distribution of the input signal to different MFGC is simplified when it is on voltage form.

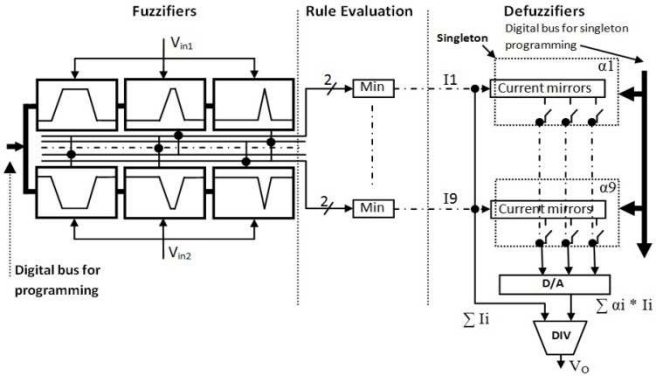

Fig. 2. Block diagram of the 2-input, 1-output, 9-rule fuzzy controller

Using these techniques several interesting CMOS fuzzifier have been reported. [4]-[7] Often in the applications which fuzzifier in transconductance mode is used, the input transconductor determine the overall linearity of the system. Modern fabrication technologies and wireless applications also require low supply voltage and low power consumption, which make it difficult to achieve transconductors with high linearity and low supply voltage over a reasonable input range.

Consequently, multiple circuit techniques have been proposed in literature to improve the linearity of MOS transconductors.[8]-[11] The reported linearization techniques include: cross-coupling of multiple differential pairs, adaptive biasing, source degeneration (using resistor or MOS transistor), shift level biasing, series connection of multiple differential pairs and pseudo-differential stages(using transistor in the triode region or in saturation).

In this paper, we report a versatile circuit for the implementation of CMOS transconductance-mode fuzzifier circuit. The circuit uses supply voltages 1.5V which significantly lower than most previous proposals. The circuit uses the source degeneration technique to improve the linearity.

Furthermore, it can be employed for all applications where

a highly accurate voltage to current conversion should be realized.

The source degeneration linearization technique has been briefly reviewed in section II and the proposed high-linear MOS transconductor is introduced in this section, also the dc transconductance characteristic of the proposed circuit is presented in this Section.

The proposed fuzzifier is presented in section III and several simulation results are presented in this section. Conclusion is presented in section IV.

II. CMOS IMPLEMENTATION OF FUZZIFIER CIRCUIT

In this section, a new circuit for the generation of trapezoidal functions is described. In the following, the proposed circuit will be presented starting from the linear transconductor used. Then, the circuitry needed to generate the trapezoidal shapes will be added.

A. Linear Transconductor Design

Considering quadratic *i* - v characteristics for the MOS transistors and neglecting the channel length modulation effect, the simple differential MOS transconductor (shown in Fig. 1) has a transfer characteristic given by:

$$i_o = \sqrt{2KI_o}\, v_i \sqrt{1 - \frac{v_i^2 K}{8I_o}} \qquad (1)$$

Where k represents the transconductance parameter ($k = \mu C_{ox} \frac{W}{L}$).

Better linearity can be achieved for large effective gate-to-source voltages $V_{GSeff} = V_{GS} - V_{TH}$. For low-voltage applications this constitutes a major drawback Furthermore, large transconductance values can be obtained only by using large bias currents and large area transistors; however this changes cause to enlarge the power consumption and active area.

One of the topologies to linearize the transfer characteristic of the MOS transconductor is the one using source degeneration resistors. However, this technique eliminates the electronic tuning capability of the Transconductor because the transconductance value is set by the degeneration resistors. Replacing the degeneration resistors by MOS transistors functioning in the triode region the circuit in Fig.3 is obtained.

Considering perfectly matched transistors and neglecting the body and channel length modulation effects, the transfer characteristic of this transconductor is given by:

$$i_o = \frac{4\beta_3\sqrt{2\beta_1 I_o}}{\beta_1 + 4\beta_3} v_i \sqrt{1 - \frac{2v_i^2 \beta_1 \beta_3^2}{I_o(\beta_1 + 4\beta_3)^2}} \qquad (2)$$

Usually, the nonlinear term under the square root can be made much smaller than unity and improved linearity and larger input dynamic range can be obtained. However, increased linearity means smaller equivalent transconductance and reduced tuning capability. The circuit has bandwidth and noise performances comparable to the simple differential pair.

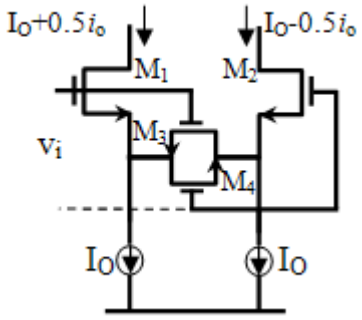

Fig. 3. MOS transconductor using source degeneration transistor in triode region

B. The novel linear MOS transconductor

We proposed a new MOS transconductor that uses the linearization approach presented above. The proposed circuit consists of 2 main blocks; a main differential pair with source degeneration resistors which the resistors are replaced by MOS transistors functioning in the triode region and low-voltage current mirrors.

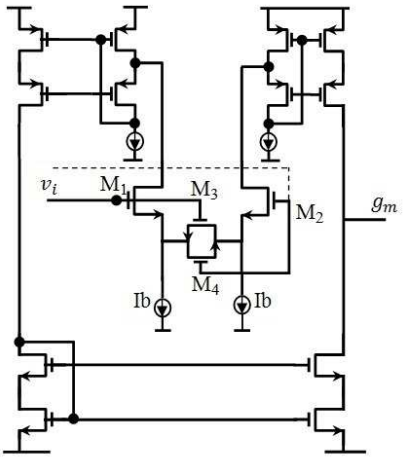

Fig. 1. The novel linear transconductor

The minimum supply voltage is limited by the path formed by I_b, M_b and M_C, so the minimum supply voltage is

$$V_{DD}^{min} = V_{GSC} + 2V_{DSbsat} \qquad (12)$$

where V_{GSC} is gate-source voltage of M_C, V_{DSbsat} is the minimum voltage drop in current source I_b and can be as small as 0.15V in 0.35µm CMOS technology, $V_{tn} = 0.65$ V for NMOS, so

$$V_{DD}^{min} = V_{tn} + 3V_{DSsat} = 0.65 + 3 \times 0.15 = 1.1\text{V}$$

We have selected V_{DD}=1.5 V in order to have an

appreciable voltage swing.

The proposed transconductor was laid out in standard 0.35µm CMOS technology. Post layout simulations from extracted circuit were performed for a 1.5 V supply using HSPICE and level 49 parameters (BSIM3V3). Fig. 4 shows DC characteristic of proposed transconductance circuit.

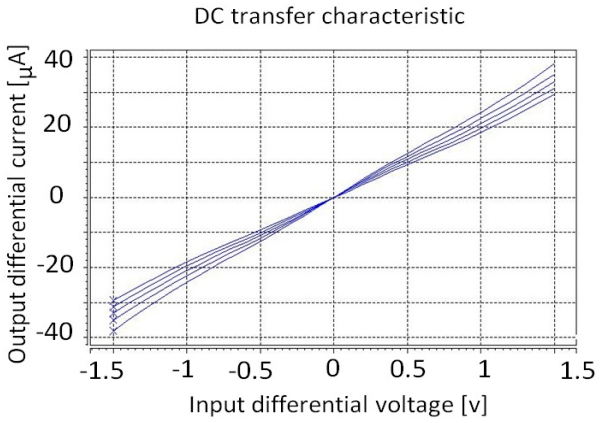

Fig. 2. Post layout simulated DC transfer characteristic

C. *Fuzzifier circuit*

Using two instances of transconductor in Fig. 4 and a minimum current selector circuit, a trapezoidal transconductor characteristic can be generated (Fig. 6):

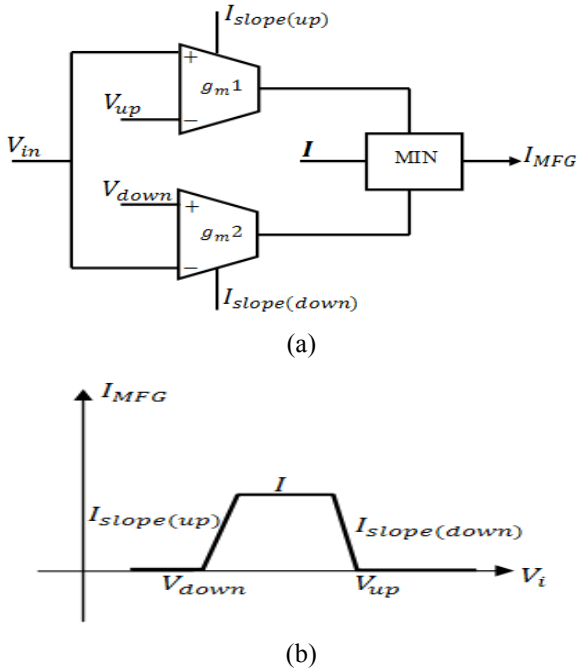

Fig. 6: (a) MFG block diagram, (b) MFG output

This block consists of two transconductors. One creates a positive ramp and the other creates a negative ramp, one defines the V_{up} and the other defines V_{down} , also each transconductor can independently define the slope of the up and down part via bias current I_b , then outputs go through a minimum current selector circuit which takes the minimum of them to construct a trapezoid output current.

The new low voltage MIN circuit is shown in Fig. 7:

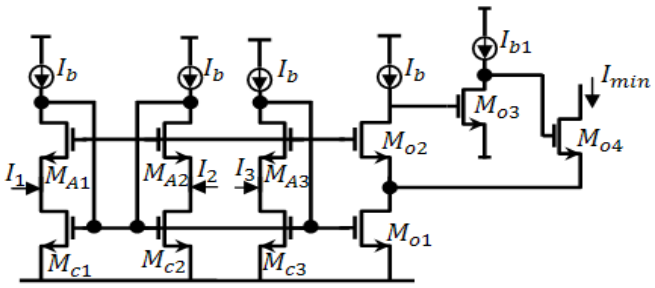

Fig. 7. MIN circuit

A proposed circuit has 3 input branches and each branch consists of a current sensing transistor M_{Ci} and a voltage follower M_{Ai} while the gates of transistors M_{Ai} are connected to a common-mode constant voltage V_b .

V_{GS} voltages of all M_{Ci} transistors are equal and proportional to minimum of input currents of I_1, I_2, I_3.this condition drive them to have different V_{DS} voltage. Since they (M_{C1}, M_{C2} and M_{C3}) have different V_{DS} voltage, the voltage follower of all branches (M_{A1}, M_{A2} and M_{A3}) are turned off with the exception of voltage follower in the loosing branch that has the minimum of input currents I_1, I_2 and I_3.

This transistor remains ON and with M_{O1}- M_{O4} formed a high performance current mirror that can copy the minimum current to the output.

This MIN circuit also defines the fuzzy one level for whole MFG circuit. By choosing the value of **I** for the fuzzy one value we also can cut the output signal at the level we want so in other words selecting **I** value, we can use the most linear part of the output signal.

III. SIMULATION

The Fuzzifier depicted in Fig. 6 was laid out in standard 0.35µm CMOS technology. Post layout simulations from extracted circuit were performed for a single 1.5 V power supply voltage using HSPICE and level 49 parameters (BSIM3V3).

Fig. 6 and Fig. 7 and Fig. 8 show SPICE simulation of the MFG. All the parameters are independently tunable.

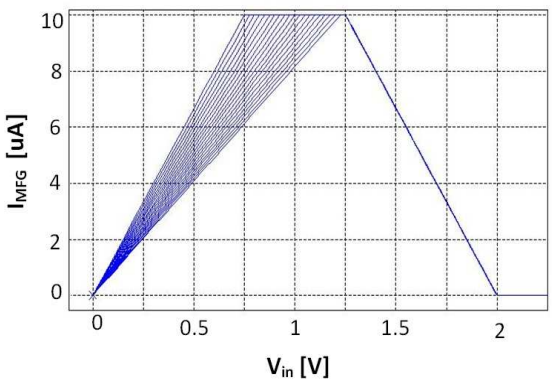

Fig. 6. MFG slope tunability

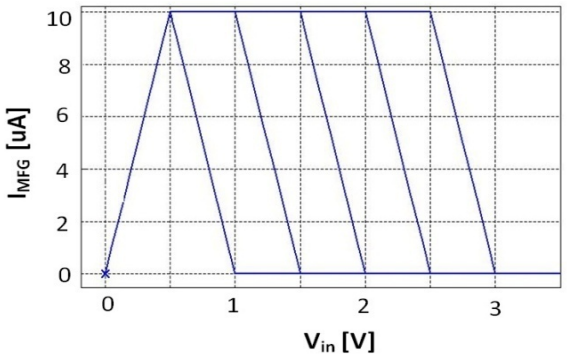

Fig. 7. MFG width tunability

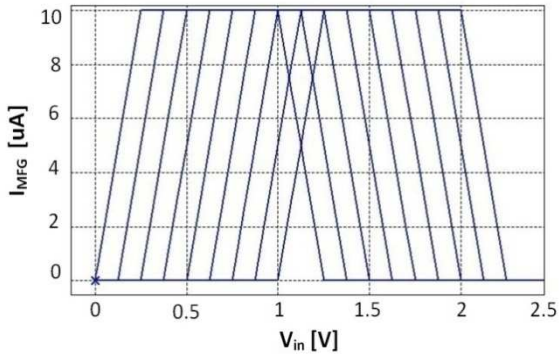

Fig. 8. MFG position tunability

IV. CONCLUSION

A novel low-voltage CMOS circuit for the Implementation of trapezoidal transconductance Functions with programmable characteristics have been introduced. The proposed circuit uses the source degeneration linearization method to achieve better linearity. The circuit can be used for the implementation of VLSI analogue neuro-fuzzy systems. The proposed circuit has independently adjustable height, slope, position, and width of the trapezoidal function and has been verified by simulation results.

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