Optimization of Switching Characterization of Inverter Design Using Artificial Neural Network

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***Abstract*– In this paper, we investigate the efficiency of artificial neural network in switching characterization of inverter design. Circuit design deals with complicated nonlinear equations. We have exploited that neural networks are capable of complicated nonlinear mapping. In this work, performance criteria of inverter employed to circuit design. The ANN based designs of inverter are compared with theoretical designs and PSO results under transient performance. Our simulations show that the designed inverters have high accuracy and optimized the switching characterization of inverter.**

***Keywords*– Artificial Neural Network, Switching Characterization, Inverter Design, Accuracy and Optimized**

I. INTRODUCTION

Revolutionary computation is an efficient tool for automated design of integrated circuits that has been one of the most important and challenging topics in VLSI design process. Demand for electronic circuit automation has increased due to complexity growth in VLSI circuits [1]. Therefore, M. Deepakaraj, in 1993 presented a detailed design methodology for soft-switched inverter [2], Blaabjerg in 1997 introduced and discussed the optimized design of a three-phase PWM-VS inverter [3], in 2010 Mo. Wei, proposed an optimal design method for two level inverters [4] and Delican used artificial bee Colony optimization considering propagation delays to CMOS inverter design [5], E. Koutroulis, in 2012 presented a methodology for the optimal design of transformerless grid-connected PV inverters [6], and Kyoo Jae Shin Designed a bike inverter using adaptive state observer of DC-link [7].

On the other hand, neural networks are strongly capable in learning and prediction which makes them an efficient tool to deal with nonlinear problems. For example, Xiao Sun in 1999 Designed and implemented a neural-network-controlled UPS inverter [8], in 2009, He Su-fen designed a three-phase photovoltaic grid connected inverter based on RBF neural network [9] and Kashif presented a voltage source inverter which is controlled with space vector pulse width modulation (SPWM) designed using three layers feed forward back propagation based artificial neural network (ANN) [10], Fan, Bo in 2010 studied and analyzed on intelligent fault diagnosis for inverting circuit and proposed an improved diagnosis method combined BP neuron network and D-S evidence theory [11], Altin, Necmi in 2011 designed an inverter as current controlled to decrease the susceptibility to phase errors, and neuro-fuzzy controller is used as current controller [12], J. Ganesh Prasad in 2012 improved power quality using Neural Network controller based cascaded H-Bridge multilevel inverter type D-STATCOM [13].

In this study, we apply Multilayer Perceptron (MLP) for inverter design. For this purpose, an inverter structure, considering dynamic characteristics, is used for designing a MLP neural network. Criteria of inverter employed to inputs of MLP neural network and outputs are parameters of inverter. The next section briefly describes the architecture of the applied network. In section 3, describes the inverter characteristics and in next section Inverter design using MLPNN is described and finally, results are given.

II. METHOD

Neural network models are used in several fields such as medicine, mathematical modeling, engineering, etc [14]. In this paper, neural network architecture is used for inverter design, then results compared with theoretical designs under transient performance. One of the most popular neural networks is feed forward MLP network by back propagation training algorithm, as shown in Fig. 1. The number of inputs and output neurons are fixed by criteria of inverter fed to network and characterizations of inverter, respectively, but the number of layers and neurons in hidden layers are not known.

As shown in Fig. 1, the activation functions of neurons in hidden layers are following sigmoidal function:

$$\emptyset(x) = \frac{1}{1+exp(-x)} \quad (1)$$

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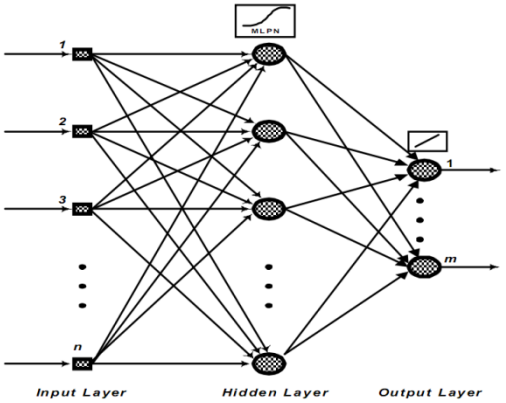

Fig. 1: The three layers of a feed forward neural network which illustrates a MLPN [15]

And the output expressed with:

$$\hat{y}_k(t) = \sum_{i=1}^{n_i} w_{jk}^2 \varnothing\left[\sum_{i=1}^{n_i} w_{ij}^1 v_i^0(t) + b_j^1\right]; \quad (2)$$

$$1 \leq k \leq m$$

Where w_{ij}^1 and w_{jk}^2 are the weights of the connection between input and hidden layer, weights of connection between hidden and output layer, respectively. b_j^1 and v_i^0 show the thresholds in hidden nodes and inputs, respectively. φ(•) is an activation function that is a sigmoidal function [16].

III. INVERTER CHARACTERISTICS

The switching characteristics of digital integrated circuits and in particular, of inverter circuits, essentially determine the overall operating speed of digital systems. The transient performance requirements of a digital system are usually among the most important design specifications that must be met by the circuit designer [1].

Therefore, the switching speed of the circuit must be estimated and optimized very early in the design phase [17], [18].

The closed-form delay expressions have been derived under the assumption of pulse excitations for lumped load capacitances. Before derivation of delay expressions, definitions of output voltage fall and rise times and propagation delay times are explained. The fall time, tf, is defined as the time required for the output voltage to drop from V90% level to V10% level. Similarly the rise time, tr, is the time required for the output voltage to rise from the V10% level to V90% level. The propagation delay times τpHL and τpLH determine the input-to-output signal delay during the high-to-low and low to high transitions of the output respectively. By definition τpHL is the time delay between the V50% transition of the rising input voltage and the V50% transition of the falling output voltage. Similarly, τpLH is defined as the time delay between the V50% transition of the falling input voltage and the V50% transition of the rising output voltage [17], [18].

Delay expressions can be obtained by solving the state equation of the output node in the time domain. In order to calculate fall time of the output voltage, output capacitance should be discharged through active NMOS transistor, as given in Fig. 2a, considering PMOS is cut-off. As seen from Fig. 2b, output fall time is calculated considering that NMOS operates in saturation mode during t1 and in linear mode during t2 - t1 time interval [1].

Accordingly, total output fall time, t2, is given as follows [17]:

$$t_f = \frac{C_L}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{DD} - V_{tn})}\left[\frac{2(V_{tn} - 0.1V_{DD})}{(V_{DD} - V_{tn})} + \ln\left(\frac{(2(V_{DD} - V_{tn})) - 0.1V_{DD}}{0.1V_{DD}}\right)\right] \quad (3)$$

In order to calculate rise time of the output voltage, output capacitance should be charged through active PMOS transistor, as given in Fig. 3a, considering NMOS is cut-off. As seen from Fig. 3b, output rise time is calculated considering that PMOS operates in saturation mode during t3 and in linear mode during t4 - t3 time interval.

Accordingly, total output rise time, t4, is given as follows [17]:

$$t_r = \frac{C_L}{\mu_p C_{ox}\left(\frac{W}{L}\right)_p (V_{DD} - |V_{tp}|)}\left[\frac{2(|V_{tp}| - 0.1V_{DD})}{(V_{DD} - |V_{tp}|)} + \ln\left(\frac{(2(V_{DD} - |V_{tp}|)) - 0.1V_{DD}}{0.1V_{DD}}\right)\right] \quad (4)$$

Analysis of propagation delay times τpHL and τpLH also involves discharging output capacitance through active NMOS and charging output capacitance through active PMOS respectively. In order to simplify the derivation of delay expressions, the input voltage waveform is usually assumed to be an ideal step pulse with zero rise and fall times. Under this assumption, τpHL becomes the time required for the output voltage to fall from VOH to the V50% level and τpLH becomes the time required for the output voltage to rise from VOL to the V50% level [17, 18].

As seen from Fig. 4, the output propagation high-to-low delay time corresponds to t6 - t5 time interval. Similarly t8 - t7 time interval is equal to the output propagation low-to-high delay time.

According to that, propagation delay times are given below [17]:

$$t_{pHL} = \frac{C_L}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{DD} - V_{tn})}\left[\frac{2V_{tn}}{(V_{DD} - V_{tn})} + \ln\left(\frac{4(V_{DD} - V_{tn})}{V_{DD}} - 1\right)\right] \quad (5)$$

$$t_{pLH} = \frac{C_L}{\mu_p C_{ox}\left(\frac{W}{L}\right)_p (V_{DD} - |V_{tp}|)}\left[\frac{2|V_{tp}|}{(V_{DD} - |V_{tp}|)} + \ln\left(\frac{4(V_{DD} - |V_{tp}|)}{V_{DD}} - 1\right)\right] \quad (6)$$

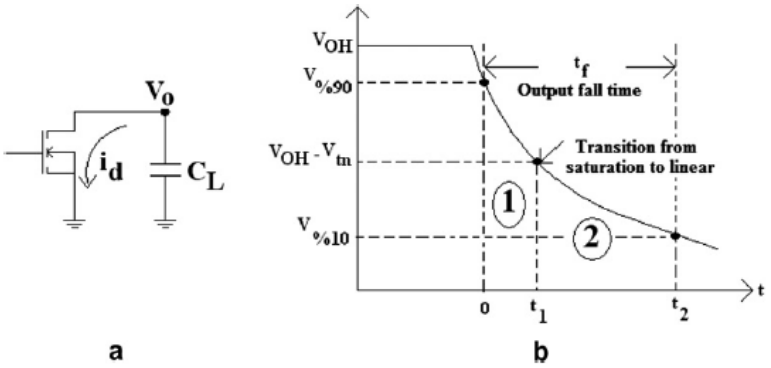

Fig. 2: (a) Load capacitance discharges through NMOS transistor, (b) Output voltage waveform during high-to-low transition [17], [18]

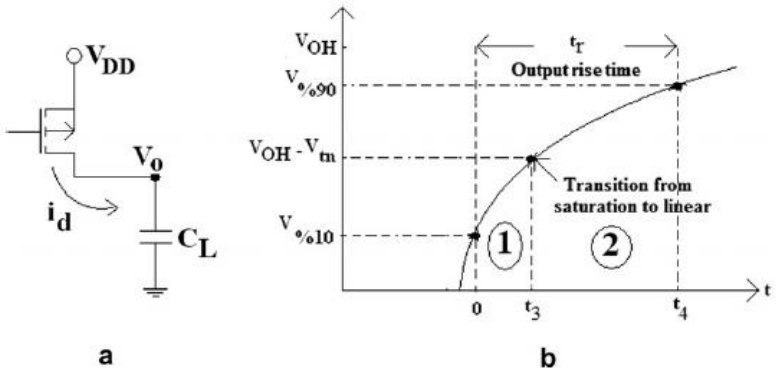

Fig. 3: (a) Load capacitance charges through PMOS transistor, (b) Output voltage waveform during low-to-high transition [17], [18]

IV. INVERTER DESIGN USING MLPNN

Revna Acar Vural in 2011 used PSO to circuit design, and the optimal circuit designed by the PSO algorithm [1]. We select the best MLP neural network with respect to results of [1]. Then the results of network compared with actual design. In order to investigate the usage of MLP neural network in inverter design, two case studies were down.

In this work, the parameters of inverter were set as $V_{dd} = 2.5\ v$, $V_{tn} = 0.3655\ v$, $|V_{tp}| = 0.5466\ v$, $\mu_n C_{ox} = 243.6\ \mu A/v^2$ and $\mu_p C_{ox} = 51.6\ \mu A/v^2$.

In study 1 for training the MLP neural network, the inputs are maximum and minimum of C_L, maximum and minimum of $(W/L)_n$, maximum and minimum of $(W/L)_p$, maximum and minimum of t_f and maximum and minimum of t_r and the outputs are C_L, $(W/L)_n$ and $(W/L)_p$ that are results of PSO algorithm in [1] also t_r and t_f that are PSPICE results. In this study, the best network obtained with three layers that layers 1, 2 and 3 contain to 10, 5 and 5 neurons, respectively. Accuracy of this network is equal to 0.95875.

In study 2 in order to MLP neural network training, the inputs are maximum and minimum of C_L, maximum and minimum of $(W/L)_n$, maximum and minimum of $(W/L)_p$, maximum and minimum of t_f, maximum and minimum of t_r, maximum and minimum of t_{pHL} and maximum and minimum of t_{pLH} and the outputs are C_L, $(W/L)_n$ and $(W/L)_p$ that are results of PSO algorithm in [1] also t_r, t_f, t_{pHL} and t_{pLH} that are PSPICE results. In this study, the best network obtained with four layers that layers 1, 2, 3 and 4 contain to 30, 20, 10 and 5 neurons, respectively. Accuracy of this network is equal to 0.98494.

V. RESULTS

The best designed MLP neural network in study 1 is shown in Fig. 4. The results of this MLPNN are error and accuracy of training, performance of test data and all data that are shown in Fig. 5.

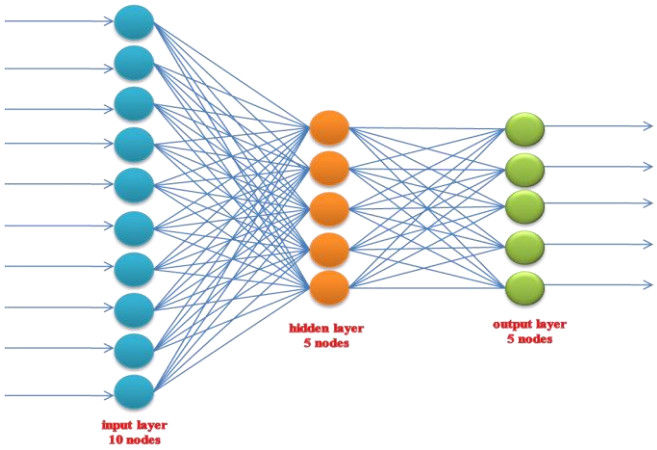

Fig. 4: The best designed MLP neural network in study 1

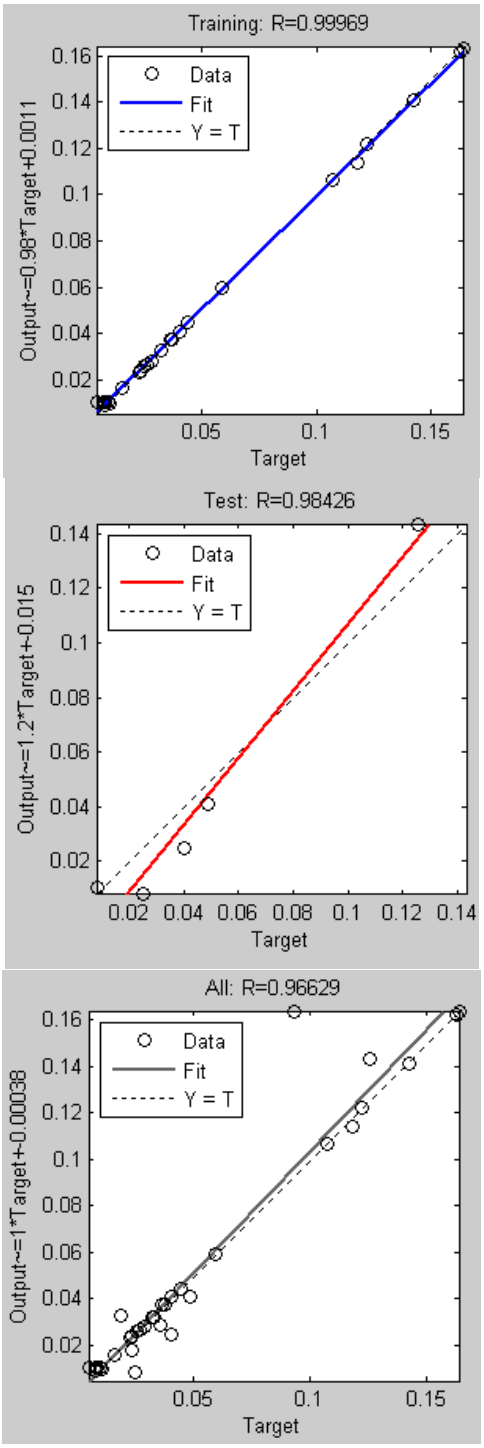

Fig. 5: Performance of training, test and all data in designed MLPNN in study 1

As shown in fig.5 performance of training, test and all data in study 1 are 0.99969, 0.98426 and 0.96629, respectively.

The ANN results in study 1, PSPICE results and PSO results in [1], are given in Table 1.

The best designed MLP neural network in study 2 is shown in Fig. 6.

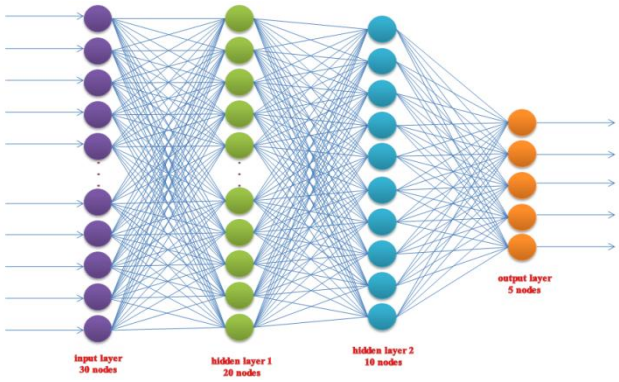

Fig. 6: The best designed MLP neural network in study

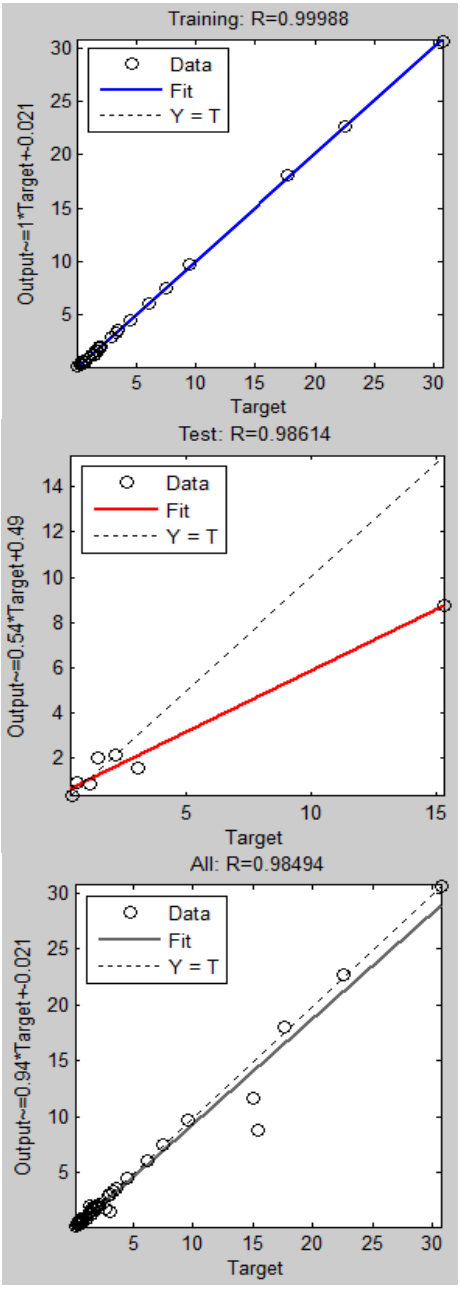

Fig. 7: Performance of training, test and all data in designed MLPNN in study 2

As shown in Fig. 7 performance of training, test and all data in study 2 are 0.99988, 0.98614 and 0.98494, respectively.

The ANN results in study 2, PSPICE results and PSO results in [1], are given in Table 2.

VI. CONCLUSIONS

This paper compared the results of a multilayer perceptron network (MLPN), particle swarm optimization algorithm (PSO) and PSPICE, to investigation of switching characterization of inverter design considering transient performance. The neural networks were capable in learning and prediction which makes them an efficient tool to deal with nonlinear problems and are easy to run.

However, The MLPN shows better results than PSO. The MLPN is simple network that results in faster convergence. The results of our estimation show significant improvement in investigation of switching characterization of inverter design. This paper has estimated specifications of inverter design in two studies with 96% and 98% accuracy, respectively.

Table 1: Comparing of proposed MLP neural network results, PSPICE results and PSO results in study 1

PSPICE inputs				PSPICE results		PSO results		MLPN results	
#	C_L	$(W/L)_n$	$(W/L)_p$	t_f	t_r	t_f	t_r	t_f	t_r
1	0.835	2.488	12.457	4.86	4.01	1.86	1.86	4.3046	3.6781
2	0.471	1.851	9.269	3.53	2.36	1.41	1.41	3.3327	2.1028
3	0.980	2.355	11.794	5.91	3.76	2.31	2.31	7.7732	2.2347
4	1.028	0.808	4.041	12.2	10.7	7.07	7.07	12.099	11.641
5	0.514	3.269	16.368	2.54	1.58	0.87	0.87	2.7464	2.1509
6	0.845	2.844	14.240	4.41	2.66	1.65	1.65	4.6583	2.8963
7	0.773	3.242	16.237	3.65	2.28	1.32	1.32	3.6223	2.3037
8	0.262	2.644	13.979	1.61	0.84	0.55	0.55	1.1379	0.6546
9	0.569	3.368	16.866	2.68	1.66	0.94	0.94	3.0335	2.0458
10	0.841	1.767	8.854	6.31	4.25	2.64	2.64	5.2199	3.5566

Table 2: Comparing of proposed MLP neural network results, PSPICE results and PSO results in study 2

PSPICE inputs				PSPICE results				PSO results				MLPN results			
#	C_L	$(W/L)_n$	$(W/L)_p$	t_f	t_r	t_{pHL}	t_{pLH}	t_f	t_r	t_{pHL}	t_{pLH}	t_f	t_r	t_{pHL}	t_{pLH}
1	0.749	3.525	17.651	3.2	1.91	1.75	0.89	1.18	1.18	0.55	0.55	3.2456	2.0032	1.5114	0.86508
2	0.403	1.900	9.515	2.97	2.01	1.58	0.87	1.18	1.18	0.55	0.55	3.1905	1.996	1.5229	0.83431
3	0.550	6.131	30.705	1.50	0.82	0.79	0.39	0.50	0.50	0.23	0.23	1.4242	0.89489	0.7754	0.487645
4	0.134	1.492	7.470	1.22	0.89	0.64	0.38	0.50	0.50	0.23	0.23	1.2200	0.90669	0.7963	0.52946
5	0.512	3.011	15.079	2.69	1.64	1.37	0.73	0.94	0.94	0.44	0.44	3.0045	1.5843	1.8456	0.73718
6	0.430	3.070	15.373	2.14	1.43	1.14	0.60	0.78	0.78	0.36	0.36	2.4823	1.5729	0.9115	0.62405
7	0.430	4.500	22.535	1.53	0.89	0.82	0.42	0.53	0.53	0.25	0.25	1.2201	1.0722	0.88848	0.66739
8	1.620	5.448	27.279	4.73	2.78	2.52	1.27	1.65	1.65	0.77	0.77	3.1102	1.9946	1.74113	0.76711
9	0.423	7.327	36.691	0.98	0.60	0.53	0.26	0.32	0.32	0.15	0.15	1.2201	1.2005	0.76161	0.22011
10	0.314	7.385	36.983	0.81	0.45	0.40	0.19	0.24	0.24	0.11	0.11	1.2201	0.5243	0.40476	0.18481

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